

7/15/3

SHEET 1 OF 1

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 240324US-2 TTC DIV		SERIAL NO. <b>101618619</b> <b>NEW APPLICATION</b>	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Tohru OZAKI, et al.			
				FILING DATE HEREWITH		GROUP Unassigned <b>2815</b>	
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
<b>JSL</b>	AA	5,281,555	01/1994	CHO	<b>438</b>	<b>625</b>	
<b>JSL</b>	AB	5,361,234	11/1994	IWASA	<b>365</b>	<b>210</b>	
<b>JSL</b>	AC	5,410,161	04/1995	NARITA	<b>257</b>	<b>41</b>	
<b>JSL</b>	AD	5,689,126	11/1997	TAKAISHI	<b>257</b>	<b>306</b>	
	AE						
	AF						
	AG						
	AH						
	AI						
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	AK						
	AL						
	AM						
	AN						
<b>FOREIGN PATENT DOCUMENTS</b>							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
<b>JSL</b>	AO	4-05-129552	05-1993	JAPAN			
<b>JSL</b>	AP	4-08-181290	07-1996	JAPAN			
<b>JSL</b>	AQ	4-11-354727	12-1999	JAPAN			
	AR						
	AS						
	AT						
	AU						
	AV						
<b>OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)</b>							
<b>JSL</b>	AW	Takashima et al., A Sub-40ns Random-Access Chain FRAM Architecture with a 7ns Cell-Plate-Line Drive, 1999, IEEE, International Solid State Circuits Conference, pp. 102, 103, 150					
<b>JSL</b>	AX	Takeshima et al., Gain Cell Block Architecture for Gigabit-Scale Chain Ferroelectric RAM, June 1999, Symposium on VLSI Circuits Digest of Technical Papers, pp. 103-04					
	AY						
	AZ						<input type="checkbox"/> Additional References sheet(s) attached
Examiner <b>JSL Echen</b>					Date Considered <b>9/1/04</b>		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							